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MC14443
MC14447

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

ANALOG-TO-DIGITAL CONVERTER LINEAR SUBSYSTEM

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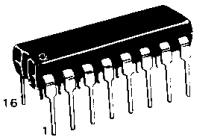
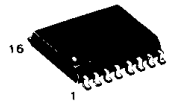
The MC14443 and the MC14447 are 6-channel, single-slope, 8-10 bit analog-to-digital converter linear subsystems for microprocessor-based data and control systems. Contained in both devices are a one-of-8 decoder, an 8-channel analog multiplexer, a buffer amplifier, a precision voltage-to-current converter, a ramp start circuit, and a comparator. The output driver of the MC14443's comparator is an open-drain N-channel which provides a sinking current. The output driver of the MC14447's comparator is a standard B-Series P-Channel, N-Channel pair.

A processor system (such as the MC68HC05 series) provides the addressing, timing, counting, and arithmetic operations required for implementing a full analog-to-digital converter system. A system made up of a processor and the linear subsystem has features such as automatic zeroing and variable scaling (weighting) of six separate analog channels.

- Quiescent Current 0.8 mA Typical at V_{DD} = 5 V
- Single Supply Operation +4.5 to +18 Volts
- Direct Interface to CMOS MPUs
- Typical Resolution — 8 Bits
- Typical Conversion Cycle as Fast as 300 μs
- Ratiometric Conversion Minimizes Error
- Analog Input Voltage Range: V_{SS} to V_{DD} — 2 V
- Chip Complexity: MC14443 — 150 FETs
  MC14447 — 151 FETs



P SUFFIX
PLASTIC DIP
CASE 648

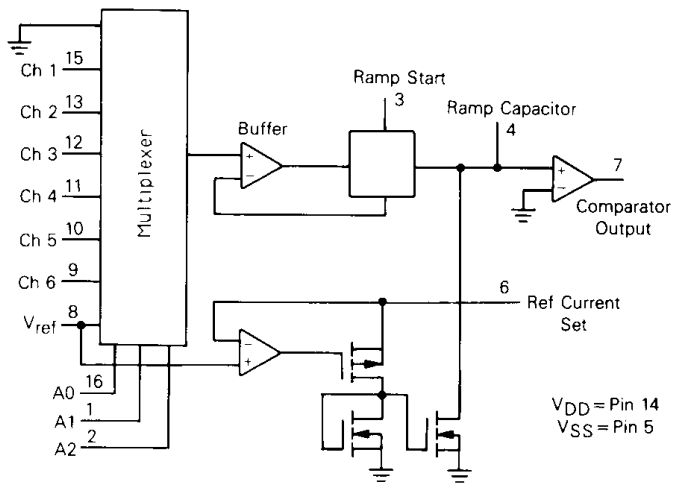


DW SUFFIX
SOG
CASE 751G

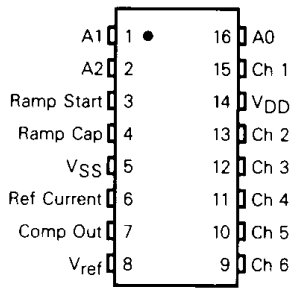
ORDERING INFORMATION

MC14443P, MC14447P	Plastic DIP
MC14443DW only	SOG Package

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ #	25°C Max	85°C Min	85°C Max	Unit
Output Voltage – Comparator "0" Level	V_{OL}	5.0	–	0.05	–	0.01	0.05	–	0.05	V
V_{in} @ Pin 4 = 0 V		10	–	0.05	–	0.01	0.05	–	0.05	
		15	–	0.05	–	0.01	0.05	–	0.05	
V_{in} @ Pin 4 = 1.0 V "1" Level	V_{OH}	5.0	4.95	–	4.95	4.99	–	4.95	–	V
(R_{pullup} = 10 kΩ, MC14443 only)		10	9.95	–	9.95	9.99	–	9.95	–	
		15	14.95	–	14.95	14.99	–	14.95	–	
Input Voltage-Address, Ramp Start "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									V
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current – Comparator	I_{OH}									mA
V_{in} @ Pin 4 = 1.0 V (MC14447 only)										
(V_{OH} = 2.5 V)		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 V)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 V)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 V)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
V_{in} @ Pin 4 = 0 V	I_{OL}									mA
(V_{OL} = 0.4 V)		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 V)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current – Address, Ramp Start	I_{in}	15	–	±0.3	–	–	±0.3	–	±1.0	μA
Input Current – Analog Inputs	I_{in}	15	–	–	–	±0.1	±50	–	–	nA
Input Capacitance – Address, Ramp Start	C_{in}	15	–	–	–	5.0	7.5	–	–	pF
V_{in} = 0 V										
Quiescent Current	I_{DD}	5	–	–	–	0.8	1.5	–	–	mA
		10	–	–	–	1.5	–	–	–	
		15	–	–	–	1.7	3.0	–	–	
Crosstalk Between Any Two Input Channels	V_{Cr}	–	–	–	–	0	4.0	–	–	mV
Reference Current Range	I_R	–	–	–	10	–	50	–	–	μA
Channel Input Voltage Range	V_{AI}	5	–	–	0	–	3.0	–	–	V
		10	–	–	0	–	8.0	–	–	
		15	–	–	0	–	13.0	–	–	
Buffer Amplifier Output Offset	V_{BO}	5	–	–	–	0.285	–	–	–	V
		10	–	–	–	0.400	–	–	–	
		15	–	–	–	0.420	–	–	–	
Comparator Threshold	V_{TC}	5	–	–	0	0.195	V_{BO}	–	–	V
		10	–	–	0	0.275	V_{BO}	–	–	
		15	–	–	0	0.290	V_{BO}	–	–	
Reference Voltage Range	V_{ref}	5	–	–	2.0	–	3.0	–	–	V
		10	–	–	2.0	–	8.0	–	–	
		15	–	–	2.0	–	13.0	–	–	
Conversion Linearity	L_C									% Full
$C > 100$ pF, V_{AI} = 0 to 2.5 V, V_{ref} = 2.5 V		5	–	–	−0.5	–	+0.5	–	–	Scale
V_{AI} = 0 to 7.0 V, V_{ref} = 7.0 V		10	–	–	−0.5	–	+0.5	–	–	
V_{AI} = 0 to 12.0 V, V_{ref} = 12.0 V		15	–	–	0.5	–	+0.5	–	–	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V	Min	Typ #	Max	Unit
Output Rise Time—Comparator (MC14447 only)	t_{TLH}	5.0	–	120	240	ns
		10	–	75	150	
		15	–	65	130	
Output Fall Time—Comparator	t_{THL}	5.0	–	250	500	ns
(R_L = 10 k to V_{DD}—MC14443)		10	–	350	700	
(R_L = ∞—MC14447)		15	–	650	1300	
Propagation Delay Time—Comparator MC14443	t_{PLH}	5.0	–	550	1100	ns
(R_L = 10 k to V_{DD})		10	–	500	1000	
		15	–	550	1100	
		5.0	–	350	700	ns
		10	–	300	600	
		15	–	300	600	
MC14447	t_{PLH}	5.0	–	600	1200	ns
		10	–	475	950	
		15	–	500	1000	
	t_{PHL}	5.0	–	450	980	ns
		10	–	540	1080	
		15	–	750	1500	
Multiplexer Propagation Delay	t_M	5.0	–	180	360	ns
		10	–	125	250	
		15	–	110	220	
Ramp Start Delay Time	t_{TS}	5.0	–	40	80	ns
		10	–	25	50	
		15	–	20	40	
Acquisition Time*	t_A	5.0	–	30	60	μs
C = 1000 pF		10	–	15	30	
R_{ref} = 100 kΩ		15	–	14	28	

* Acquisition Time includes multiplexer propagation delay, ramp start propagation delay and the time required to charge ramp capacitor to the selected input voltage.

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PIN DESCRIPTIONS

A2, A1, A0, ANALOG MUX ADDRESS INPUTS (PINS 2, 1, 16) — These inputs determine the input voltage source to be presented to the measurement system according to the Truth Table shown in Figure 2.

Ramp Start, RAMP START (PIN 3) — When Ramp Start is low, the ramp capacitor is charged to a voltage associated with the selected input channel. When Ramp Start is brought high, the connection to the input channel is broken and the capacitor begins to ramp toward V_{SS}. See Figure 4.

Ramp Cap, RAMP CAPACITOR (PIN 4) — The ramp capacitor is used to generate a time period when discharged from a selected voltage via a precise reference current. A polystyrene or mylar capacitor is recommended. The value should be ≥ 100 pF so that the board and stray capacitances have negligible effects. Large values of capacitance with the associated large leakage currents are not recommended because the leakage current must be insignificant in comparison to the minimum reference current (10 μA).

V_{SS}, NEGATIVE POWER SUPPLY (PIN 5) — This is system ground.

Ref Current, REFERENCE CURRENT (PIN 6) — To discharge the ramp capacitor, the reference current is fixed via a resistor (R_{ref}) to a positive supply from Pin 6. Typical current is equal to $(V_{DD} - V_{ref})/R_{ref}$.

Comp Out, COMPARATOR OUTPUT (PIN 7) — This output is low when the capacitor has reached the discharged voltage and is high otherwise. The MC14443 requires a pull-up resistor on Pin 7 due to the open-drain configuration. The MC14447 does not require a pull-up resistor.

V_{ref}, REFERENCE VOLTAGE (PIN 8) — This is the known voltage to which the unknown is compared.

INPUT CHANNELS (PINS 9, 10, 11, 12, 13, 15) — Input channels 1 through 6 are used to monitor up to six separate unknown voltages. Selection is via the address inputs.

V_{DD}, POSITIVE POWER SUPPLY (PIN 14) — This pin is the package positive power supply pin.

FIGURE 1 – VOLTAGE TO PULSE WIDTH CONVERSION

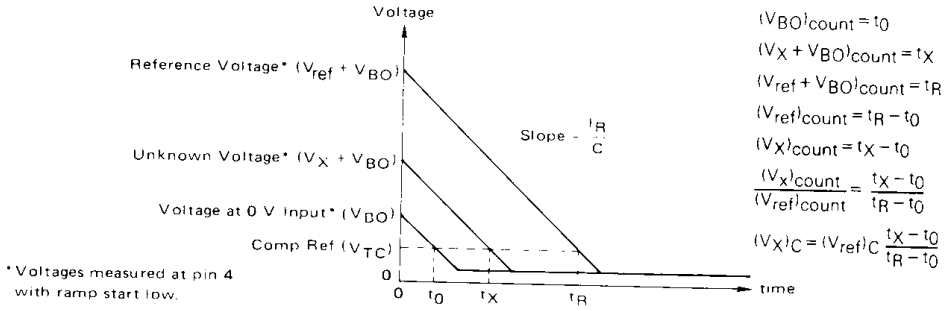

FIGURE 2 – TRUTH TABLE

A2	A1	A0	Input Selected	
0	0	0	V_{SS}	Channel 0 (ground)
0	0	1	Ch1	Channel 1
0	1	0	Ch2	Channel 2
0	1	1	Ch3	Channel 3
1	0	0	Ch4	Channel 4
1	0	1	Ch5	Channel 5
1	1	0	Ch6	Channel 6
1	1	1	V_{ref}	Channel 7 (External Reference)

FIGURE 3 – TYPICAL APPLICATIONS CIRCUIT

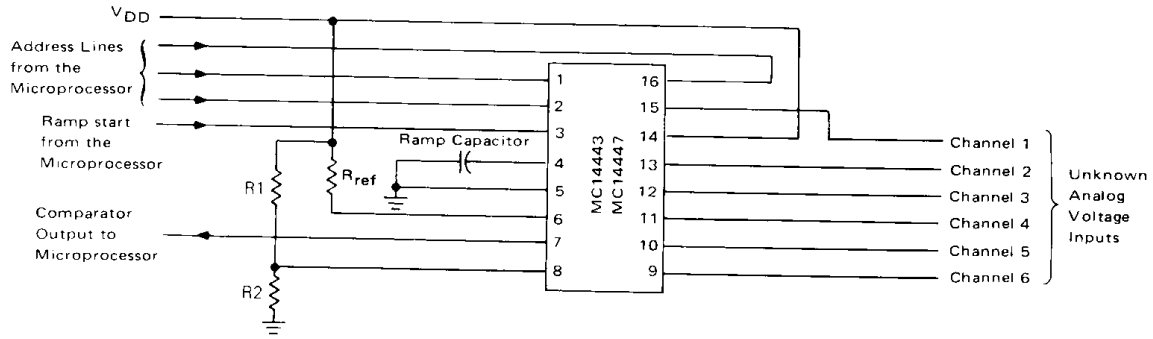

FIGURE 4 – SOFTWARE FLOW (CONVERSION SEQUENCE)

Step No.	A2	A1	A0	Ramp Start	Comment
1.	1	1	1	0	Channel 7 Selected (Reference Voltage)
2.	1	1	1	1	Record time until Pin 7 goes low
3.	0	0	0	0	Channel 0 Selected (Ground)
4.	0	0	0	1	Record time until Pin 7 goes low
5.	0	0	1	0	Channel 1 Selected
6.	0	0	1	1	Record time until Pin 7 goes low
Calculate $t_{Ch7} - t_{Ch0} = t_{Ch7}'$ Step 2–Step 4					
Calculate $t_{Ch1} - t_{Ch0} = t_{Ch1}'$ Step 6–Step 4					
Calculate $V_{unknown} = V_{Ch7}(t_{Ch1}'/t_{Ch7}')$*					
7.	0	1	0	0	Channel 2 Selected
8.	0	1	0	1	Record time until Pin 7 goes low
Calculate $t_{Ch2} - t_{Ch0} = t_{Ch2}'$					
Calculate $V_{unknown} = V_{Ch7}(t_{Ch2}'/t_{Ch7}')$†					
etc.					

*Weighting of the analog signal on Channel 1.
†Weighting of the analog signal on Channel 2.

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APPLICATION INFORMATION FOR 10-BIT RESOLUTION

DETERMINING R_{ref} AND C_{ramp}

The maximum time for the ramp capacitor to discharge from the largest voltage (V_{ref}) is equal to the time required to fill a 10-bit counter. An MPU such as the MC146805E2, running at 5 MHz, could fill the counter in about 1.8 ms; i.e.,

LOOP INC COUNT	3 cycles
TST PIA	3
BNZ LOOP	3
	9 cycles

$$t = 1024 \times 9 \text{ cycles} \times 200 \text{ ns/cycle} = 1.843 \text{ ms}$$

For $V_{DD} = 5$ V and $V_{ref} = 2.5$ V:

$C = I_R(t)/V_{ref}$ where I_R = reference current, t = time, V_{ref} = reference voltage

$C_{max} = (50\ \mu A)\ (1.843\ ms)/2.5\ V = 0.037\ \mu F$

$C_{min} = (10\ \mu A)\ (1.843\ ms)/2.5\ V = 0.0074\ \mu F$

Choose $C_{ramp} = 0.022\ \mu F$ with a reference current of 30 μA. Use a polystyrene capacitor.

$R_{ref} = (V_{DD} - V_{ref})/I_R = (5 - 2.5)/30 = 83\ k\Omega$

choose 82 kΩ for R_{ref}

DETERMINING THE TOTAL CONVERSION TIME

Mux prop delay, t_M	360 ns
Ramp start prop delay, t_{TS}	80 ns
Comparator prop delay, $t_{PLH/HL}$	1200 ns
Capacitor discharge time	1.843 ms
Capacitor charge time, use 150 μA for charging current	0.366 ms*
Approx. total time	2.2 ms

*Ramp start must be low at least 0.366 ms for this example.

ACQUIRING 10 BITS OF RESOLUTION

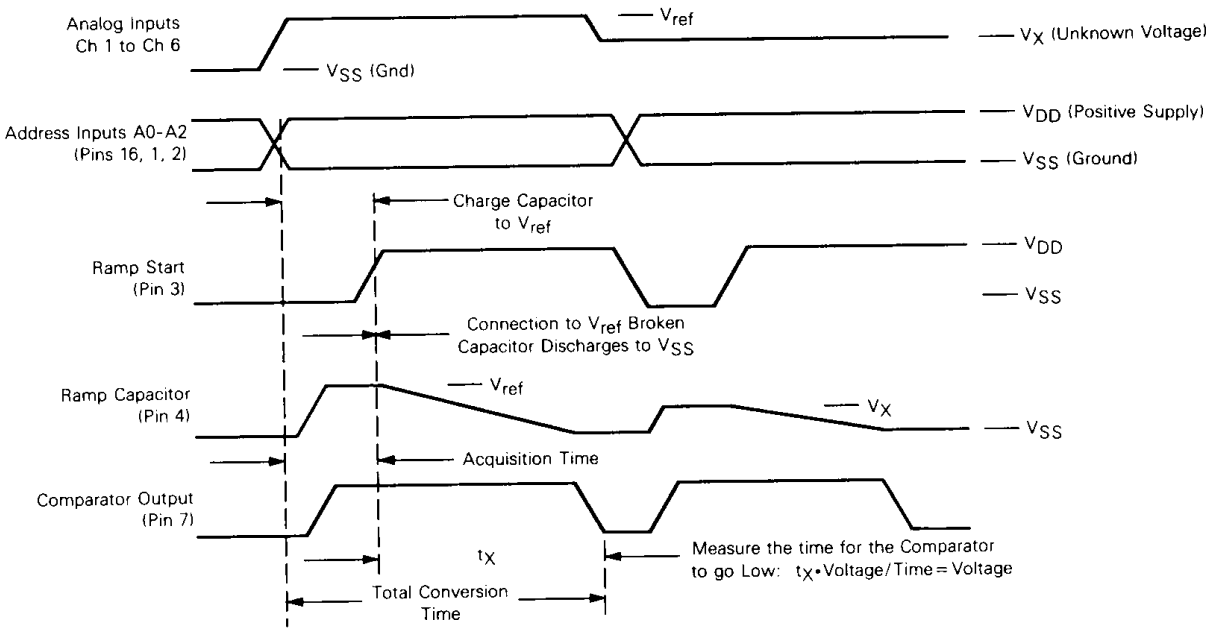
For 10 bits of resolution, the MPU must perform 2^{10} or 1024 counts during the longest A/D conversion discharge cycle. Therefore, 1.843 ms/1024 = 1.8 μs/bit. For ±1 LSB of accuracy, the MPU must sample the signal at pin 7 every 1.8 μs; this is a sample rate of 555 ks/s.

For a 2.5 V reference, the resolution per bit is 2.5 V/1024 = 2.44 mV/bit. Therefore, the 2.5 V reference must have < 2.44 mV of noise.

If the MC14443/7 is maintained near 25°C, the nonlinearity is ±0.5% of the full scale reading.

A 0.1 μF shunting capacitor at the supply pins is recommended.

TIMING DIAGRAM



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