TOSHIBA

Unit in mm

7.85~8.80

11-10C4

TOSHIBA PHOTOCOUPLER GaAlAs IRED & PHOTO IC

6N138, 6N139

CURRENT LOOP DRIVER.

LOW INPUT CURRENT LINE RECEIVER.

CMOS LOGIC INTERFACE.

The TOSHIBA 6N138 and 6N139 consists of a GaA ℓ As infrared emitting diode coupled with a split-Darlington output configuration. A high speed GaA ℓ As IRED manufactured with an unique LPE junction, has the virtue of fast rise and fall time at low drive current.

Isolation Voltage: 2500V_{rms} (Min.)

Current Transfer Ratio

: 6N138 - 300% (Min.) ($I_F = 1.6mA$)

: 6N139 - 400% (Min.) ($I_F = 0.5 \text{mA}$)

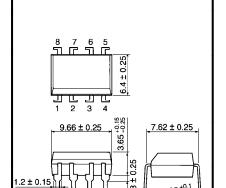
Switching Time: 6N138 - tpHL=10μs (Max.)

- t_{PLH} = 35 μs (Max.)

 $6N139 - t_{PHL} = 1 \mu s \text{ (Max.)}$

- $tp_{IH} = 7\mu s$ (Max.)

• UL Recognized: UL1577, File No. E67349



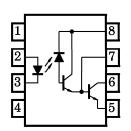
Weight: 0.54g

TOSHIBA

2.54 ± 0.25

PIN CONFIGURATION (Top view)

 $0.5 \pm 0.$



1 : N.C.

2: ANODE

3 : CATHODE

11-10C4

4 : N.C.

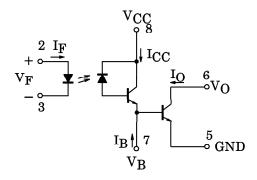
5 : GND

6: OUTPUT

7: OUTPUT BASE

8 : V_{CC}

SCHEMATIC



961001EBC2

1/5

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

MAXIMUM RATINGS (*) (Ta = 0°C to + 70°C)

	CHARACTERISTIC	SYMBOL	RATING	UNIT	
LED	Forward Current	(Note 1)	$I_{\mathbf{F}}$	20	mA
	Pulse Forward Current		I _{FP} (*1)	40	mA
	Total Pulse Forward Current	I _{FP} (*2)	1	Α	
	Reverse Voltage	v_{R}	5	V	
	Diode Power Dissipation	(Note 2)	P_{D}	35	mW
OR	Output Current	(Note 3)	IO	60	mA
T	Emitter-Base Reverse Voltage		$ m V_{EB}$	0.5	V
EC	Supply Voltage		V _{CC} (*3)	-0.5 to 18	V
DET	Output Voltage	VO (*3)	-0.5 to 18	V	
	Output Power Dissipation	(Note 4)	PO	100	mW
Ope	erating Temperature Range	$T_{ m opr}$	0 to 70	°C	
Storage Temperature Range			$\mathrm{T_{stg}}$	-55 to 125	°C
Lea	d Solder Temperature (10s) (*4)	T_{sol}	260	°C	
Isolation Voltage (1min., R.H.≤60%)				2500	V_{rms}
			BVS (**)	3540	v_{dc}

- (*) JEDEC Registered Data
- (**) Not Registered JEDEC
- (*1) 50% duty cycle, 1ms pulse width
- (*2) Pulse width 1μ s, 300pps
- (*3) $6N138 \cdots -0.5$ to 7V
- (*4) 1.6mm below seating plane

Gallium arsenide (GaAs) is a substance used in the products described in this document. GaAs dust and fumes are toxic. Do not break, cut or pulverize the product, or use chemicals to dissolve them. When disposing of the products, follow the appropriate regulations. Do not dispose of the products with other industrial waste or with domestic garbage.

The products described in this document are subject to foreign exchange and foreign trade control laws.

The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.

The information contained herein is subject to change without notice.

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED TEMPERATURE (Ta = 0°C to 70°C, Unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	(*5) TYP .	MAX.	UNIT	
Current Transfer	6N139	CTR (*)	I_{F} =0.5mA, V_{O} =0.4V V_{CC} =4.5V	400	800	_	- %	
Ratio (Note 5, 6)			$I_{\rm F}$ =1.6mA, $V_{\rm O}$ =0.4 V	500	900			
	6N138		$V_{CC} = 4.5V$	300	600	_		
	6N139	$v_{ m OL}$	$ I_{\rm F}=1.6{ m mA},\ I_{ m O}=6.4{ m mA} $ $V_{ m CC}=4.5{ m V}$	_	0.1	0.4	- V	
I I Outunt			I _F =5mA, I _O =15mA V _{CC} =4.5V	_	0.1	0.4		
Logic Low Output Voltage (Note 6)			$I_F=12mA$, $I_O=24mA$ $V_{CC}=4.5V$	_	0.2	0.4		
	6N138		I _F =1.6mA, I _O =4.8mA V _{CC} =4.5V	_	0.1	0.4		
Logic High Output	6N139	I _{OH} (*)	$I_F=0$ mA, $V_O=V_{CC}=18V$		0.05	100		
Current (Note 6)	urrent (Note 6) 6N138		$I_F=0$ mA, $V_O=V_{CC}=7$ V	_	0.05	250	$\mu \mathbf{A}$	
Logic Low Supply Current (Note 6)		I_{CCL}	$egin{array}{l} I_{\mathbf{F}} = 1.6 \mathrm{mA}, \ V_{\mathbf{O}} = \mathrm{Open} \\ V_{\mathbf{CC}} = 5 \mathrm{V} \end{array}$	_	0.2	_	mA	
Logic High Supply Current (Note 6)		ICCH	I _F =0mA, V _O =Open, V _{CC} =5V	_	10	_	nA	
Input Forward Voltage V		V _F (*)	I _F =1.6mA, Ta=25°C	_	1.65	1.7	V	
Input Reverse Breakdown Voltage BVR		BV _R (*)	$I_R = 10 \mu A, Ta = 25$ °C	5	_	_	V	
Temperature Coefficient of Forward Voltage $ \Delta V_F / $		ΔV _F /ΔTa	I _F =1.6mA	_	-1.9	_	mV/°C	
Input Capacitance C _{IN}		$c_{\rm IN}$	$f=1MHz, V_F=0$	_	60	_	pF	
Resistance (Input-Output) R _{I-O}		R _{I-O}	$V_{\text{I-O}} = 500 \text{V (Note 7)}, \\ \text{R.H.} \le 60\%$	_	10^{12}	_	Ω	
Capacitance (Input-0	Capacitance (Input-Output)		f=1MHz (Note 7)	_	0.6	_	pF	

^(**) JEDEC Registered Data. (*5) All typicals at Ta=25°C and $V_{\hbox{\footnotesize{CC}}}\!=\!5V,$ Unless otherwise noted.

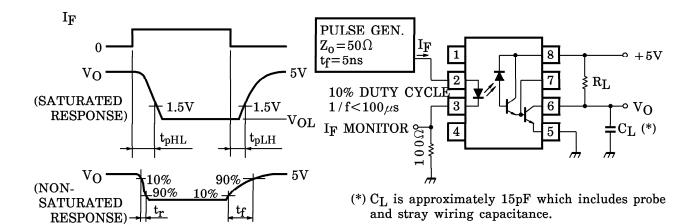
SWITCHING SPECIFICATIONS (Ta = 25°C, V_{CC} = 5V, unless otherwise specified)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay	6N139	t _{pHL} (*)	1	I_F =0.5mA, R_L =4.7k Ω	_	5	25	με
Time to Logic Low				$I_{ m F}$ =12mA, $R_{ m L}$ =270 Ω	_	0.2	1	
at Output (Note 6, 8)	Note 6, 8) 6N138			$I_F=1.6$ mA, $R_L=2.2$ k Ω	_	1	10	
Propagation Delay	6N138	t _{pLH} (*)	1	$I_F=0.5$ mA, $R_L=4.7$ k Ω	_	5	60	μs
Time to Logic High				$I_F=12mA, R_L=270\Omega$	_	1	7	
at Output (Note 6, 8)	6N139			$I_F=1.6$ mA, $R_L=2.2$ k Ω	_	4	35	
Common Mode Transic Immunity at Logic Hig Level Output (1	CM_{H}	2	I_F =0mA, R_L =2.2k Ω V_{CM} =400 V_{p-p}	_	500	_	V/μs	
Common Mode Transic Immunity at Logic Lov Level Output (N	CM_{L}	2	$\begin{split} & I_{F}\!=\!1.6\text{mA} \\ & R_{L}\!=\!2.2\text{k}\Omega \\ & V_{CM}\!=\!400V_{p\text{-}p} \end{split}$	_	-500	_	V/μs	

(*)JEDEC Registered Data.

- (Note 1) Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.
- (Note 2) Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.
- (Note 3) Derate linearly above 25°C free-air temperature at a rate of 0.7mA/°C.
- (Note 4) Derate linearly above 25°C free-air temperature at a rate of 2.0mW/°C.
- (Note 5) DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, IO, to the forward LED input current, IF, times 100%.
- (Note 6) Pin 7 Open.
- (Note 7) Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
- (Note 8) Use of a resistor between pin 5 and 7 will decrease gain and delay time.
- (Note 9) Common mode transient immunity in Logic High level is the maximum tolerable (positive) dv_{CM}/dt on the leading edge of the common mode pulse, V_{CM} , to assure that the output will remain in a Logic High state (i.e., $V_{O}\!>\!2.0V)$. Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dv_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a Logic Low state (i.e., $V_{O}\!<\!0.8V)$.

TEST CIRCUIT 1.



TEST CIRCUIT 2.

