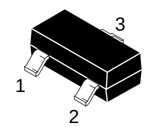
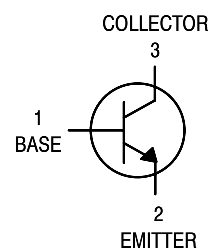
General Purpose Transistors
NPN Silicon

MMBT2222LT1
MMBT2222ALT1*

***ON Semiconductor Preferred Device**



CASE 318–08, STYLE 6
SOT–23 (TO–236)



MAXIMUM RATINGS

Rating	Symbol	2222	2222A	Unit
Collector–Emitter Voltage	V_{CEO}	30	40	Vdc
Collector–Base Voltage	V_{CBO}	60	75	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	6.0	Vdc
Collector Current — Continuous	I_C	600		mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board(1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate,(2) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

DEVICE MARKING

MMBT2222LT1 = M1B; MMBT2222ALT1 = 1P

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	MMBT2222 MMBT2222A	$V_{(BR)CEO}$	30 40	— —	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	MMBT2222 MMBT2222A	$V_{(BR)CBO}$	60 75	— —	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	MMBT2222 MMBT2222A	$V_{(BR)EBO}$	5.0 6.0	— —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	MMBT2222A	I_{CEX}	—	10	nAdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 50 Vdc, I_E = 0, T_A = 125°C) (V_{CB} = 60 Vdc, I_E = 0, T_A = 125°C)	MMBT2222 MMBT2222A MMBT2222 MMBT2222A	I_{CBO}	— — — —	0.01 0.01 10 10	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	MMBT2222A	I_{EBO}	—	100	nAdc
Base Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	MMBT2222A	I_{BL}	—	20	nAdc

1. FR–5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

March, 2001 – Rev. 1

Publication Order Number:
MMBT2222LT1/D

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 0.1 mAdc, V_{CE} = 10 Vdc)			35	—	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)			50	—	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)			75	—	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = –55°C) only	MMBT2222A		35	—	
			100	300	
(I_C = 150 mAdc, V_{CE} = 10 Vdc) (3)			50	—	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc) (3)			30	—	
(I_C = 500 mAdc, V_{CE} = 10 Vdc) (3)	MMBT2222		40	—	
	MMBT2222A				
Collector–Emitter Saturation Voltage (3)		$V_{CE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)	MMBT2222		—	0.4	
	MMBT2222A		—	0.3	
(I_C = 500 mAdc, I_B = 50 mAdc)	MMBT2222		—	1.6	
	MMBT2222A		—	1.0	
Base–Emitter Saturation Voltage (3)		$V_{BE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)	MMBT2222		—	1.3	
	MMBT2222A		0.6	1.2	
(I_C = 500 mAdc, I_B = 50 mAdc)	MMBT2222		—	2.6	
	MMBT2222A		—	2.0	

SMALL–SIGNAL CHARACTERISTICS

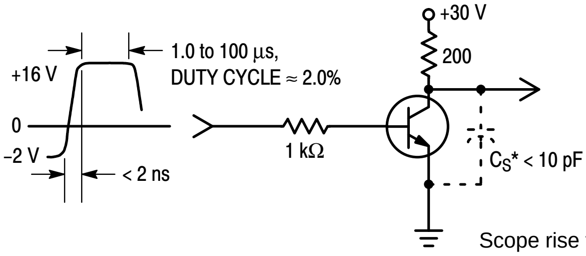
Current–Gain — Bandwidth Product (4) (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	 MMBT2222 MMBT2222A	f_T	 250 300	 — —	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	 —	 8.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	 MMBT2222 MMBT2222A	C_{ibo}	 — —	 30 25	pF
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	 MMBT2222A MMBT2222A	h_{ie}	 2.0 0.25	 8.0 1.25	kΩ
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	 MMBT2222A MMBT2222A	h_{re}	 — —	 8.0 4.0	$X\ 10^{-4}$
Small–Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	 MMBT2222A MMBT2222A	h_{fe}	 50 75	 300 375	—
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	 MMBT2222A MMBT2222A	h_{oe}	 5.0 25	 35 200	μmhos
Collector Base Time Constant (I_E = 20 mAdc, V_{CB} = 20 Vdc, f = 31.8 MHz)	 MMBT2222A	rb, C_c	 —	 150	ps
Noise Figure (I_C = 100 μAdc, V_{CE} = 10 Vdc, R_S = 1.0 kΩ, f = 1.0 kHz)	 MMBT2222A	NF	 —	 4.0	dB

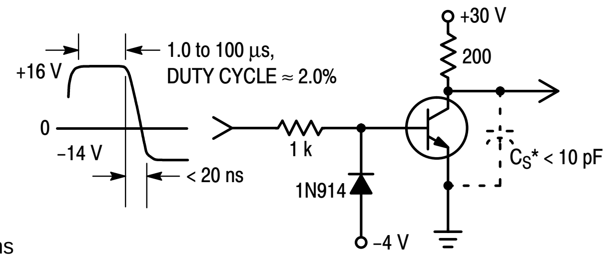
SWITCHING CHARACTERISTICS (MMBT2222A only)

Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = –0.5 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc)	t_d	—	10	ns
Rise Time		t_r	—	25	
Storage Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc)	t_s	—	225	ns
Fall Time		t_f	—	60	

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
4. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

SWITCHING TIME EQUIVALENT TEST CIRCUITS





Scope rise time < 4 ns
*Total shunt capacitance of test jig, connectors, and oscilloscope.

Figure 1. Turn–On Time **Figure 2. Turn–Off Time**

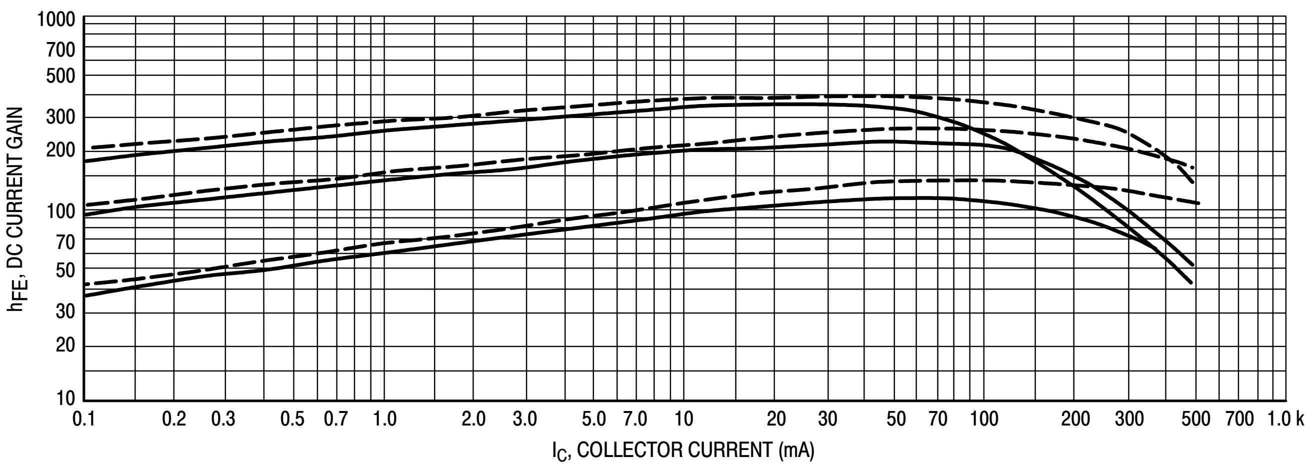


Figure 3. DC Current Gain

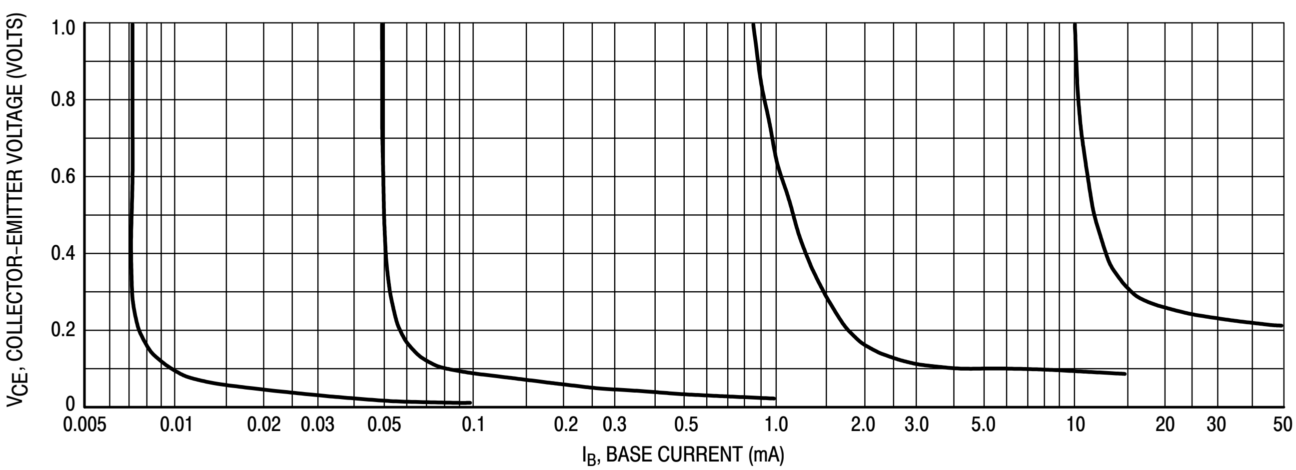


Figure 4. Collector Saturation Region

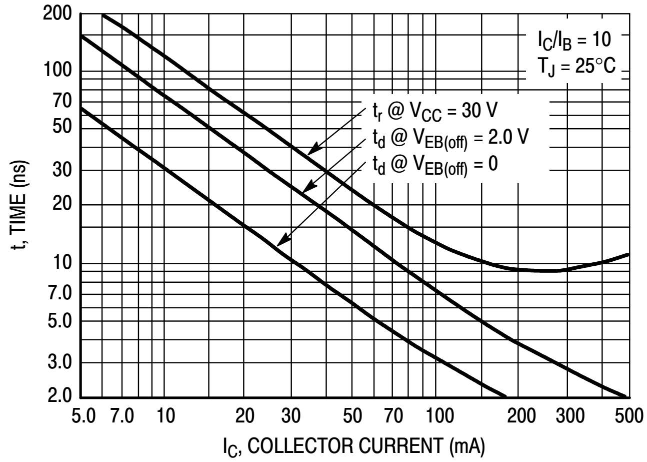


Figure 5. Turn−On Time

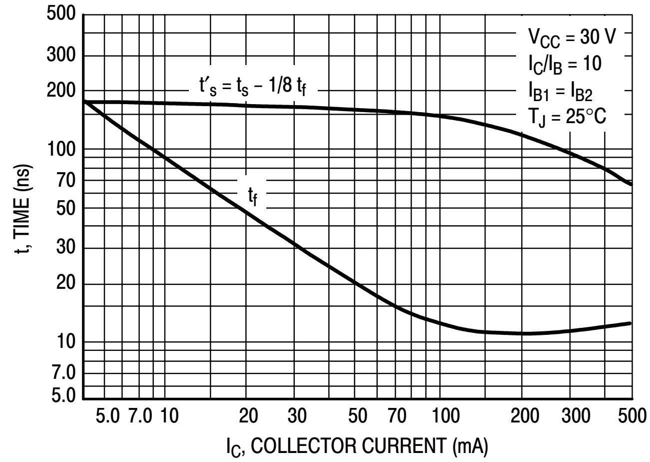


Figure 6. Turn−Off Time

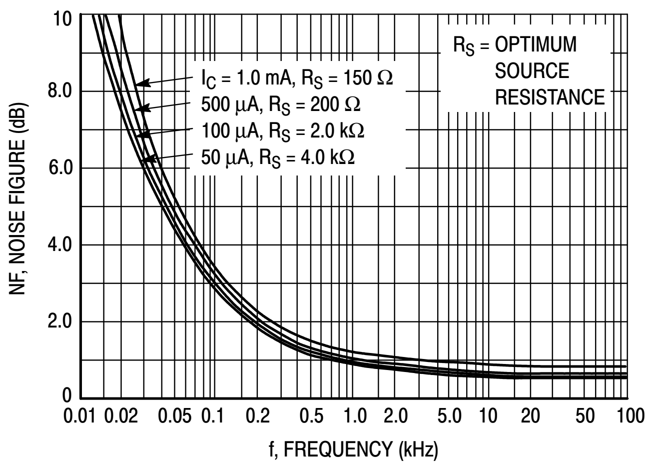


Figure 7. Frequency Effects

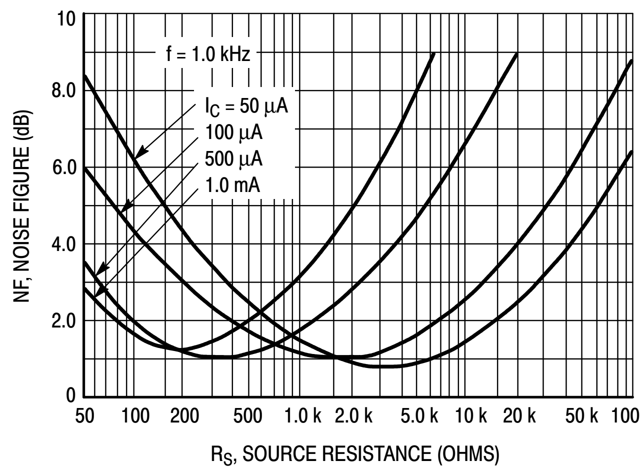


Figure 8. Source Resistance Effects

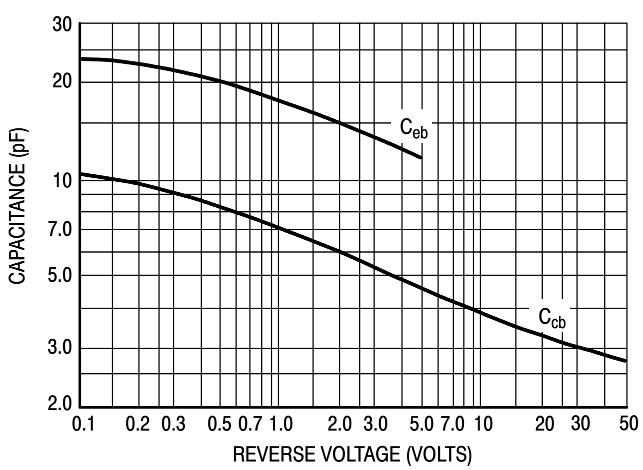


Figure 9. Capacitances

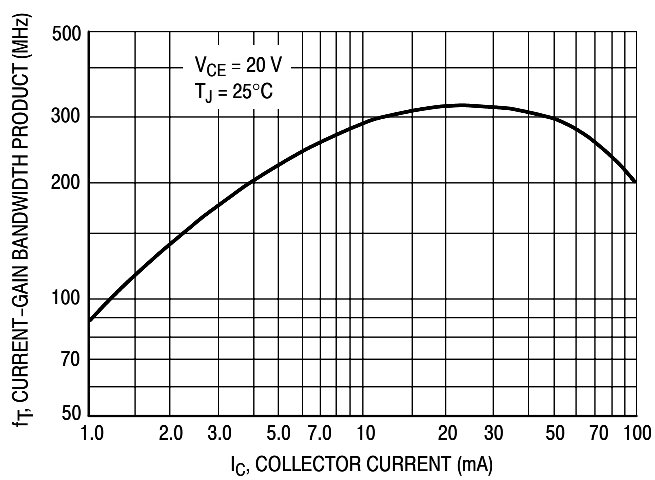


Figure 10. Current−Gain Bandwidth Product

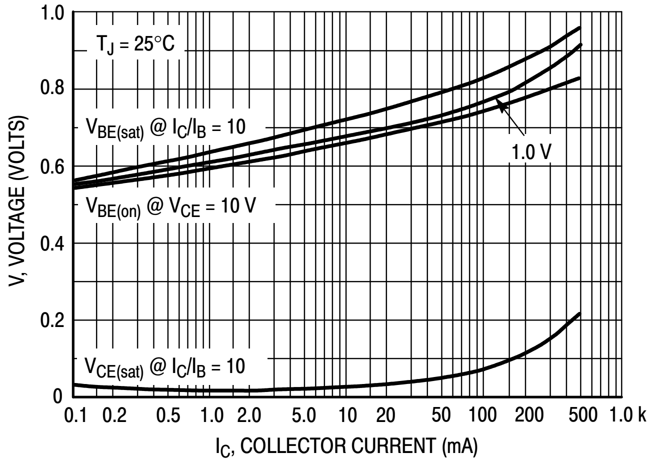


Figure 11. “On” Voltages

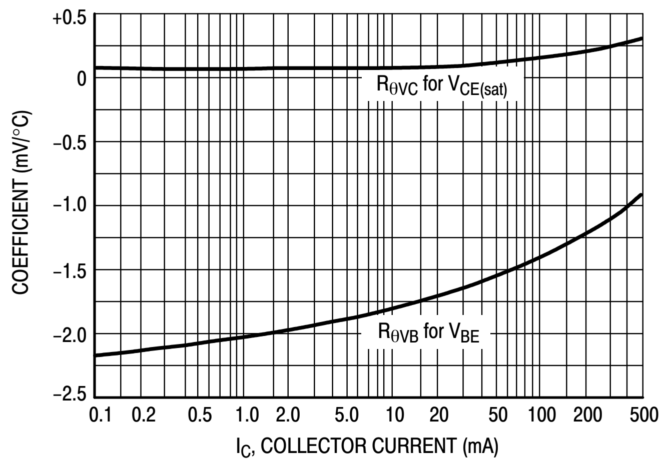
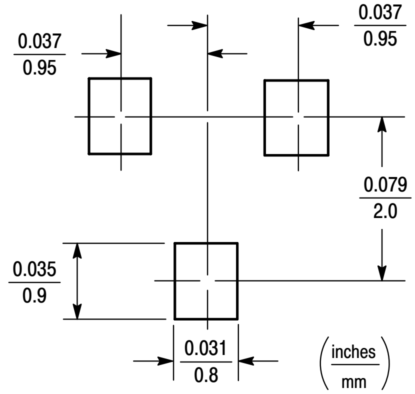


Figure 12. Temperature Coefficients

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

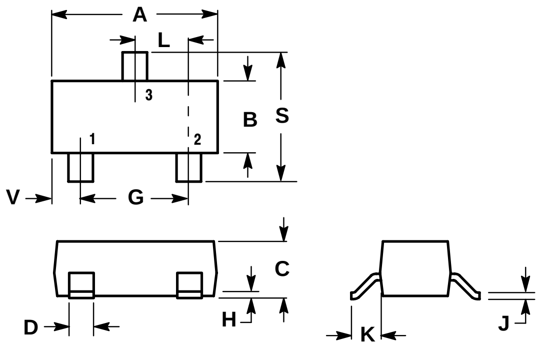
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

SOT–23 (TO–236)
CASE 318–08
ISSUE AF



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

Thermal Clad is a trademark of the Bergquist Company.

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