

# TC4501BP

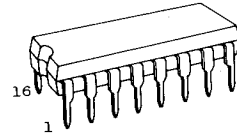
C<sup>2</sup>MOS DIGITAL INTEGRATED CIRCUIT  
SILICON MONOLITHIC

TC4501BP TRIPLE GATE (Dual 4-Input NAND Gate and 2-Input NOR/OR Gate or 8-Input AND/NAND Gate)

The TC4501BP is a combined gate which contains dual 4-input NAND gate and 2-input NOR/OR gate in one package.

Since all the outputs of these gates are provided with the buffers of inverters, the input/output transmission characteristics have been improved and the noise immunity has been elevated. Further, an increase in propagation delay time caused by an increase in load capacity is kept to a minimum.

The TC4501BP can be used as 8-input positive AND/NAND gate by externally connecting the output of NAND gate to the input of NOR/OR gate.

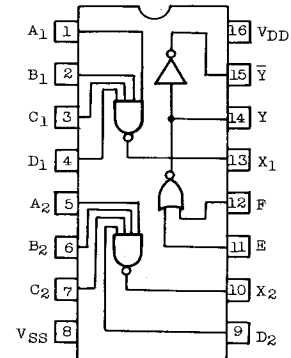


DIP16(3D16A-F)

### ABSOLUTE MAXIMUM RATINGS

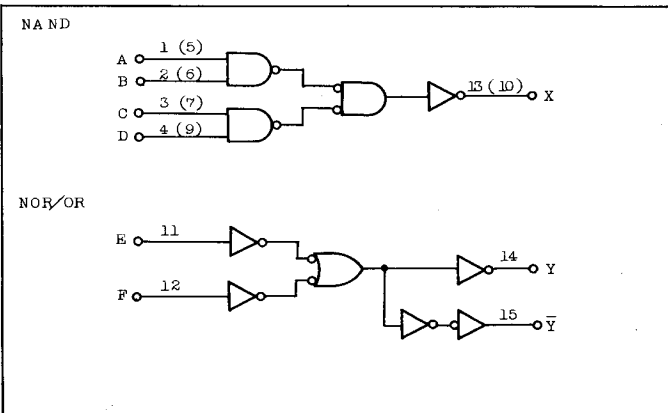
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V <sub>DD</sub>	V <sub>SS</sub> - 0.5 ~ V <sub>SS</sub> + 20	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> - 0.5 ~ V <sub>DD</sub> + 0.5	V
Output Voltage	V <sub>OUT</sub>	V <sub>SS</sub> - 0.5 ~ V <sub>DD</sub> + 0.5	V
DC Input Current	I <sub>IN</sub>	±10	mA
Power Dissipation	PD	300	mW
Operating Temperature Range	T <sub>A</sub>	-40 ~ 85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 ~ 150	°C
Lead Temp./Time	T <sub>sol</sub>	260°C · 10 sec	

### PIN ASSIGNMENT



(TOP VIEW)

### LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V<sub>SS</sub>=0V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V <sub>DD</sub>	3	-	18	V
Input Voltage	V <sub>IN</sub>	0	-	V <sub>DD</sub>	V

STATIC ELECTRICAL CHARACTERISTICS (V<sub>SS</sub>=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V <sub>DD</sub> (V)	-40°C		25°C			85°C		UNITS	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Output Voltage	V <sub>OH</sub>	I <sub>OUT</sub>   < 1μA V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	4.95	-	4.95	5.00	-	4.95	-	V	
			10	9.95	-	9.95	10.00	-	9.95	-		
			15	14.95	-	14.95	15.00	-	14.95	-		
Low-Level Output Voltage	V <sub>OL</sub>	I <sub>OUT</sub>   < 1μA V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	-	0.05	-	0.00	0.05	-	0.05	V	
			10	-	0.05	-	0.00	0.05	-	0.05		
			15	-	0.05	-	0.00	0.05	-	0.05		
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> =4.6V V <sub>OH</sub> =2.5V V <sub>OH</sub> =9.5V V <sub>OH</sub> =13.5V V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA	
			5	-2.5	-	-2.1	-4.0	-	-1.7	-		
			10	-1.5	-	-1.3	-2.2	-	-1.1	-		
			15	-4.0	-	-3.4	-9.0	-	-2.8	-		
			15	-4.0	-	-3.4	-9.0	-	-2.8	-		
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> =0.4V V <sub>OL</sub> =0.5V V <sub>OL</sub> =1.5V V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	0.61	-	0.51	1.5	-	0.42	-	mA	
			10	1.5	-	1.3	3.8	-	1.1	-		
			15	4.0	-	3.4	15.0	-	2.8	-		
			15	4.0	-	3.4	15.0	-	2.8	-		
Input High Voltage	V <sub>IH</sub>	V <sub>OUT</sub> =0.5V, 4.5V V <sub>OUT</sub> =1.0V, 9.0V V <sub>OUT</sub> =1.5V, 13.5V  I <sub>OUT</sub>   < 1μA	5	3.5	-	3.5	2.75	-	3.5	-	V	
			10	7.0	-	7.0	5.5	-	7.0	-		
			15	11.0	-	11.0	8.25	-	11.0	-		
			15	11.0	-	11.0	8.25	-	11.0	-		
Input Low Voltage	V <sub>IL</sub>	V <sub>OUT</sub> =0.5V, 4.5V V <sub>OUT</sub> =1.0V, 9.0V V <sub>OUT</sub> =1.5V, 13.5V  I <sub>OUT</sub>   < 1μA	5	-	1.5	-	2.25	1.5	-	1.5	V	
			10	-	3.0	-	4.5	3.0	-	3.0		
			15	-	4.0	-	6.75	4.0	-	4.0		
			15	-	4.0	-	6.75	4.0	-	4.0		
Input Current	"H" Level	I <sub>IH</sub>	V <sub>IH</sub> =18V	18	-	0.1	-	10 <sup>-5</sup>	0.1	-	1.0	μA
	"L" Level	I <sub>IL</sub>	V <sub>IL</sub> =0V	18	-	-0.1	-	-10 <sup>-5</sup>	-0.1	-	-1.0	
Quiescent Device Current	I <sub>DD</sub>	V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub> *	5	-	0.25	-	0.001	0.25	-	3.8	μA	
			10	-	0.5	-	0.001	0.5	-	7.5		
			15	-	1.0	-	0.002	1.0	-	15		

\* All valid input combinations.

# TC4501BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V<sub>SS</sub>=0V, C<sub>L</sub>=50pF)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V <sub>DD</sub> (V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (Low to High)		t <sub>T LH</sub>		5	-	80	200	ns
				10	-	50	100	
				15	-	40	80	
Output Transition Time (High to Low)		t <sub>T HL</sub>		5	-	80	200	
				10	-	50	100	
				15	-	40	80	
NAND	Propagation Delay Time (Low to High)	t <sub>p LH</sub>		5	-	80	260	
				10	-	50	140	
				15	-	40	100	
NAND	Propagation Delay Time (High to Low)	t <sub>p HL</sub>		5	-	80	260	
				10	-	50	140	
				15	-	40	100	
NOR	Propagation Delay Time (Low to High)	t <sub>p LH</sub>		5	-	100	230	
				10	-	50	130	
				15	-	40	90	
NOR	Propagation Delay Time (High to Low)	t <sub>p HL</sub>		5	-	100	230	
				10	-	50	130	
				15	-	40	90	
NOR-Inverter	Propagation Delay Time (Low to High)	t <sub>p LH</sub>		5	-	130	260	
				10	-	70	140	
				15	-	50	100	
NOR-Inverter	Propagation Delay Time (High to Low)	t <sub>p HL</sub>		5	-	130	260	
				10	-	70	140	
				15	-	50	100	
Input Capacitance		C <sub>IN</sub>			-	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

