MOTOROLA

SEMICONDUCTORS

MC14411

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

BIT RATE GENERATOR

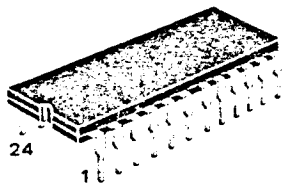
BIT RATE GENERATOR

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

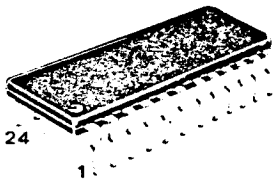
A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

- Single 5.0 Vdc (±5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 MHz)
- Sixteen Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 21
- Internal Pullup Resistor on Reset Input



L SUFFIX
CERAMIC PACKAGE
CASE 623

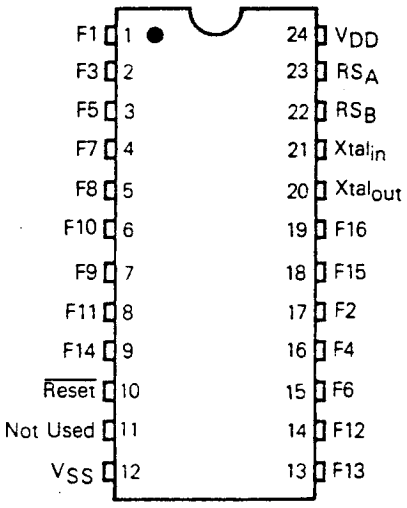


P SUFFIX
PLASTIC PACKAGE
CASE 709

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12.)

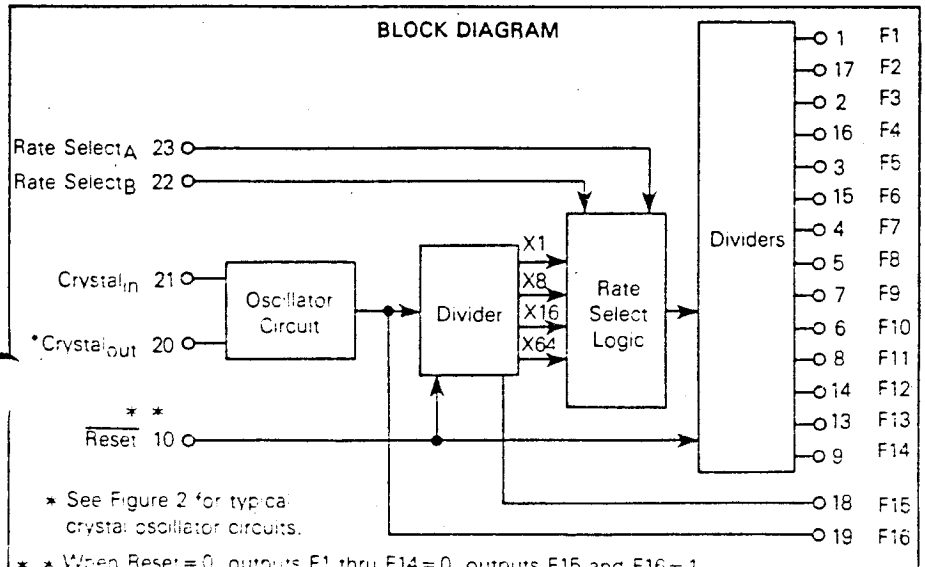
Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	5.25 to −0.5	V
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} − 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

PIN ASSIGNMENT



V_{DD} = Pin 24
V_{SS} = Pin 12

BLOCK DIAGRAM



* See Figure 2 for typical crystal oscillator circuits.

* * When Reset = 0, outputs F1 thru F14 = 0, outputs F15 and F16 = 1.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	−85°C Min	−85°C Max	Unit
Supply Voltage	V_{DD}	–	4.75	5.25	4.75	5.0	5.25	4.75	5.25	V
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	V
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	V
Input Voltage (V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
(V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
Output Drive Current (V_{OH} = 2.5 V) Source	I_{OH}	5.0	−0.23	–	−0.20	−1.7	–	−0.16	–	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mA
Input Current Pins 21, 22, 23	I_{in}	–	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Pin 10		5.0	–	–	−1.5	–	−7.5	–	–	μA
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q	5.0	–	2.5	–	0.015	2.5	–	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0			$P_D = (7.5\ mW/MHz)\ f + P_Q$					mW
Output Rise Time** $t_r = (3.0\ ns/pF)\ C_L + 25\ ns$	t_{TLH}	5.0	–	–	–	70	200	–	–	ns
Output Fall Time** $t_f = (1.5\ ns/pF)\ C_L + 47\ ns$	t_{THL}	5.0	–	–	–	70	200	–	–	ns
Input Clock Frequency	f_{CL}	5.0	–	1.85	–	–	1.85	–	1.85	MHz
Clock Pulse Width	$t_{W(C)}$	–	200	–	200	–	–	200	–	ns
Reset Pulse Width	$t_{W(R)}$	–	500	–	500	–	–	500	–	ns

†For dissipation at different external capacitance (C_L) refer to corresponding formula:
$P_T(C_L = P_D + 2.6 \times 10^{-3}(C_L - 15\ pF)\ V_{DD}{}^2 f$
where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.
**The formula given is for the typical characteristics only.

TABLE 1 — OUTPUT CLOCK RATES

Rate Select B	Rate Select A	Rate
0	0	X1
0	1	X8
1	0	X16
1	1	X64

Output Number	Output Rates (Hz) X64	X16	X8	X1
F1	614.4 k	153.6 k	76.8 k	9600
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	115.2 k	28.8 k	14.4 k	1800
F7	76.8 k	19.2 k	9600	1200
F8	38.4 k	9600	4800	600
F9	19.2 k	4800	2400	300
F10	12.8 k	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6 k	921.6 k	921.6 k	921.6 k
F16*	1.843 M	1.843 M	1.843 M	1.843 M

*F16 is buffered oscillator output.

FIGURE 1 — DYNAMIC SIGNAL WAVEFORMS

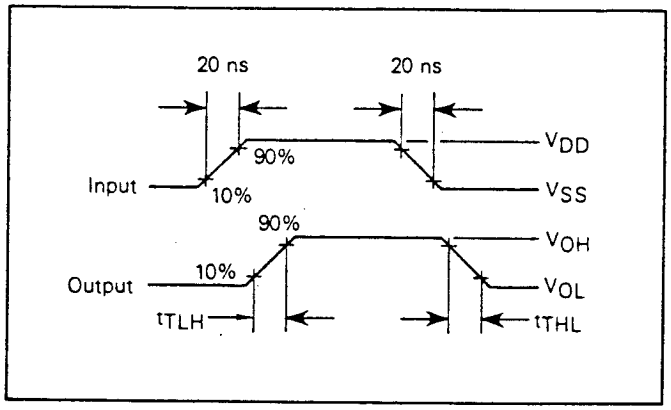
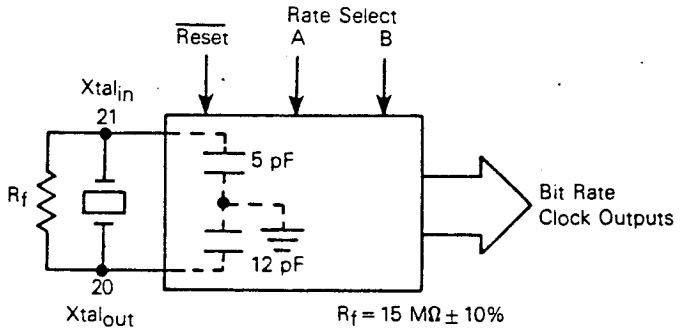


FIGURE 2 — TYPICAL CRYSTAL OSCILLATOR CIRCUIT



Crystal Specifications

Crystal Mode	Parallel
Frequency	1.8432 MHz ±0.05% @ 13 pF
R_S	540 Ω max
C_0	7.0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS — 330/TSM or Equivalent

*Suggested Crystal Suppliers:
Tyco, CTS Knights

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc., or others.

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